REMARKS

Claims 8-13, 15-19, 21, and 24-35 are presented for further examination. Claims 8, 15, 19, 24-28, and 32 have been amended. Claims 14, 22, and 23 have been canceled.

Applicants submit this corrected Amendment wherein the recitation in clam 1 on a "single" coating has been removed. Applicants believe this limitation is unnecessarily limiting, and that corrected claim 1 is allowable for the reasons argued herein.

In the Office Action mailed May 29, 2007, the Examiner rejected claims 8-13, 19, and 21 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,719,069 ("Sparks '069") in view of U.S. Patent No. 5,531,121 ("Sparks '121"). Claims 14-18 and 22-35 were rejected as anticipated by Sparks '121.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

Claim 8 is directed to a structure formed in a substrate of monolithic semiconductor material, the structure comprising at least one trench formed in the substrate having an open top and open bottom and a coating on the lateral walls of the at least one trench with material resistant to etching; a cavity having at least one wall formed below each at least one trench in communication with the open bottom of the at least one trench, and a coating formed on the at least one wall of the cavity with material inhibiting epitaxial growth; and an epitaxial layer formed on the substrate to cover the open top of the at least one trench and to encase the at least one trench and the cavity in the substrate.

In claim 8 it is noted that the substrate of semiconductor material is a monolithic substrate of semiconductor material. The monolithic nature of the wafer of monocrystalline silicon is described at page 5, line 8 of the application as filed.

Sparks '121 describes an oxide layer 42 coating the walls of a cavity 22 and a polysilicon layer 36 imposed over the oxide layer 42. Thus, Sparks '121 teaches a cavity having multiple coatings on the walls thereof. And, as the Examiner noted, Sparks '121 does not disclose an epitaxial monocrystalline layer for which the Examiner relies upon the Sparks '069 patent. The combination of Sparks '069 and Sparks '121 fails to teach, suggest, or disclose the structure recited in claim 8. More particularly, Sparks '121 does not teach or suggest a structure having a trench, a cavity, coatings on the trench and on the cavity, and a semiconductor layer closing the open top of the trench

as affirmed by the Examiner. In fact, in order to cite all of the elements, the Examiner refers to different figures of Sparks '121, which show the structure at different steps so that the above combination is never present.

For example, the Examiner cites Figures 2C, 4A, and 6 for the trench. However, Figures 2C and 4A show the trench and the cavity but no coatings and no semiconductor top layer to close the trench. Figure 6 (which is an alternative to the above figures) shows the trench, the cavity, and multiple coatings (in fact, a same coating for the cavity and the trench, and not two different coatings as set forth in the claims, *i.e.*, a coating on the trench with material resistant to etching, and a coating on the at least one wall of the cavity with material inhibiting epitaxial growth), and Sparks '121 has no semiconductor top layer to close the trench. Figures 7 and 10 of Sparks '121 have no trench (the former trenches are filled by the filling material), no open top and no open bottom.

Furthermore, Sparks '121 has no semiconductor top layer as recited in claim 8. The silicon layer 36 in Figure 4B cited by the Examiner to close the top of the trench also fills the trenches so that no open top and bottom exists.

Sparks '069 describes a structure wherein the substrate is not monolithical but formed by two bonded wafers (see the region 20, of either silicon or glass, that is bonded to the substrate 18, column 8, lines 7-15).

The Examiner cannot make a patchwork of different figures showing subsequent steps or alternative embodiments to demonstrate anticipation or obviousness of the claimed structure. This is neither reasonable nor permissible. Thus, for this reason, the combination of Sparks '121 and Sparks '069 cannot obviate the structure recited in claim 8.

Moreover, it would not be obvious to one of ordinary skill to combine Sparks '069 with Sparks '121 because Sparks '069 has no trenches, no coatings, and is obtained through a different technique that leads only to the specific structure taught therein. In particular, it is not possible to separate the teaching of forming the top layer of monocrystalline silicone from the entire teaching of Sparks '069 and to insert it into the structure of Sparks '121. In fact, the top layer of Sparks '069 is inherently tied to the specific technique to obtain it, *i.e.*, a double-wafer structure wherein the trenches and the epitaxial layer inhibiting coating have no meaning. This is not compatible with the teaching of Sparks '121.

For the foregoing reasons, applicants respectfully submit that claim 8 is clearly allowable. Dependent claims 9-13 are allowable for the features recited therein as well as for the reasons why claim 8 is allowable. More particularly, nowhere do the cited references teach or suggest a plurality of trench and cavity pairs formed in the substrate with the construction recited in claim 8 or at different levels within the substrate. Moreover, there is no teaching or suggestion of varying the trench and cavity pair to have different cross-sectional configurations, different cross-sectional sizes, and a combination of the foregoing features.

Independent claim 15 is directed to a monolithic wafer of semiconductor material. Claim 15 further recites a plurality of buried cavities formed in and completely surrounded by the semiconductor material, each cavity of the plurality of buried cavities having at least one wall formed with a single coating of a layer of material inhibiting epitaxial growth. Nowhere is there any teaching or suggestion in Sparks '069 or Sparks '121 or in any combination of these references of a cavity having at least one wall with only a single coating of a layer of material inhibiting epitaxial growth that is completely surrounded by the monolithic semiconductor material. Rather, Sparks '121 teaches two coatings, and Sparks '069 teaches a substrate that is not monolithical but formed by two bonded wafers, as discussed above. For these reasons, applicants respectfully submit that claim 15 is allowable. Dependent claims 16-18 are also allowable for the reasons discussed above with respect to claim 15 as well as for the features recited within these dependent claims.

Independent claim 19 is directed to a structure formed in monolithic semiconductor material having a cavity formed in the monolithic semiconductor material with an open top and a wall with a single coating formed of a layer of material inhibiting epitaxial growth, and a membrane formed of epitaxial growth on the monolithic semiconductor material that covers the open top of the cavity in the substrate, the membrane having a thickness in the range of between 1 and 3 μm. Applicants respectfully submit that independent claim 19 and dependent claims 21, and 24-27 are allowable in view of the discussion above with respect to claims 8 and 15.

Independent claim 28 is directed to a monolithic wafer of monocrystalline semiconductor material comprising a plurality of buried cavities, each cavity completely surrounded by the monolithic monocrystalline material and having walls covered with a single coating formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned adjacent to and

separated from each other by dividers. Independent claim 32 also recites a monolithic wafer of monocrystalline semiconductor material that comprises a plurality of buried cavities, each cavity completely surrounded by the monocrystalline material and having walls covered with a single coating formed of a layer of material inhibiting epitaxial growth, the plurality of buried cavities positioned at different heights within the wafer of monocrystalline semiconductor material. Applicants respectfully submit that these claims and all claims depending therefrom, *i.e.*, claims 29-31 which depend from claim 28, and claims 33-35, which depend from claim 32, are all allowable in view of the discussion above.

In view of the foregoing, applicants respectfully submit all of the claims in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/E. Russell Tarleton/
E. Russell Tarleton
Registration No. 31,800

ERT:jl

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

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